Abstract of the Disclosure

A new Delay Locked Loop (DLL) circuit is interoperable with products having different applications by controlling the count of a DLL circuit according to the operating clock frequency. Therefore, the products having different applications can be manufactured in the same manufacturing processes and test processes. The DLL circuit includes: a clock buffer for receiving an external clock signal; a first frequency divider for dividing the buffered clock signal; a phase detector for detecting phase error; a DLL controller for generating shift-control signals; a delay line for locking between an internal clock signal and an external clock signal; a second frequency divider for dividing the internal clock signal; and a replica unit for modeling tAC path.